Our research pertains to finding either new or more efficient methods of hardware verification, which means determining a process that can figure out whether a circuit contains a bug or not and figuring out how to fix the error. This is done by creating algebraic equations from the Boolean model of the circuit at certain cuts within the circuit itself.

There has been a good amount of success in this field in the past, but the main goal is to improve on what there is by finding methods that will reduce the time of the process. A specific goal would be finding a way to reduce the residual out of the equations formulated from the current methods, which just means find a way to tell if any of the terms in the equation equal zero, so that way we can eliminate them to decrease the amount of computation.

The methods known uses forms of rewriting, which redefine the algebraic equations cut by cut and compare it to the other form of rewriting (forward vs backward) to see if there is a difference or not.